Remarks/Arguments

Reconsideration of this application is requested.

Request for Continued Examination

In response to the final Office Action mailed on January 7, 2005, a Request for Continued Examination (RCE) is enclosed with this amendment.

Claim Status

Claims 6-10 and 12-15 were previously pending. Claims 6, 9, 13 and 14 are amended, claims 10 and 15 are canceled, without prejudice, and new claims 16-19 are added. Hence, claims 6-9, 12-14 and 16-19 are now pending.

Claim Rejections - 35 USC 102(b)

Claims 6-9 and 13-15 are rejected under 35 USC 102(b) as anticipated by Gupta (USP 5,567,648). In response, independent claim 6 is amended to clearly distinguish over Gupta. In addition, dependent claims 9, 13 and 14 are amended to emphasize additional distinctions over Gupta.

The present invention is directed to a method for preventing electrostatic damage to integrated circuit elements of a semiconductor chip package during storage. This is accomplished by electrically connecting the terminals, which are connected to the integrated circuit elements, to each other such that the terminals are in a short-circuited state. In this manner, high voltage from sources such as static electricity is applied between the short circuited terminals only and not to the integrated circuit elements. When the package is mounted to a printed circuit board, these connections are disabled either by melting conductive solder lines connecting solder balls (claim 6), or by cutting wires connecting pin-shaped terminals (new claim 16). In this manner, the terminals are in a short-circuited state, thereby preventing damage to the integrated circuit elements to which the terminals are connected, until such time immediately before the package is mounted on a printed circuit board. On mounting to the circuit board, the electrical connection between the terminals is disabled such that operation of the semiconductor chip is not obstructed.

Gupta, by contrast, does not disclose a method in which integrated circuit elements connected to terminals of a semiconductor chip package are protected from electrostatic damage prior to mounting on a printed circuit board. Rather, Gupta provides a preformed sheet 30 that is used for forming interconnect bumps, such as solder bumps, on a substrate. Preformed sheet 30 is provided with discs 36 interconnected by connecting members or ligaments 32. Preformed sheet 30 is formed, for example, from sheets of solder by roll punching. The thickness of preform sheet 30 is approximately 1 to 15 mils. A polymer backsheet thinly coated with flux may be attached to preform sheet 30.

To form interconnect bumps on a substrate 40, preformed sheet 30 is arranged on substrate 40 such that discs 36 are aligned over bond pads 42. Preformed sheet 30 is heated and melted, causing the molten metal of ligaments 32 to form hemispherical-shaped interconnect bumps 50 on bond pads 42 of substrate 40.

Importantly, Gupta's preformed sheet 30 is not a semiconductor chip package and contains no integrated circuit elements connected to its "terminals" (discs 36) that are in need of protection from electrostatic protection. Rather, it is a thin sheet of metal with a polymer backsheet. Discs 36 and ligaments 32 comprise the solder that will ultimately be used as the terminals on the substrate 40. Notably, after the solder of preformed sheet 30 is applied to substrate 40, the terminals of substrate 40 are not short circuited and therefore will not be prevented from electrostatic damage before mounting on a circuit board, as is provided by applicant's invention.

Independent claim 6 is amended to emphasize this distinction. Claim 6, as amended, requires that integrated circuit elements be connected to the terminals of the semiconductor chip package, and that these terminals be short circuited before mounting on a circuit board. Gupta's short-circuited "terminals" are not connected to any integrated circuit elements before its described mounting processes, and therefore cannot anticipate independent claim 6. Dependent claims 7-9 and 12-14 share these distinctions and are similarly allowable.

Dependent claim 9 has been amended to emphasize another aspect of the invention. Claim 9, as amended, recites:

> forming a conductive thin film on surfaces of the terminals, areas between the terminals and peripheral areas of a bottom surface of the package

Hence, rather than connecting the terminals by line-like solder members, the terminals are connected by a thin film 32 (Fig. 3) formed on the bottom surface of the package. The thin film covers the surfaces of the terminals 2, the areas between the terminals 2 and the peripheral areas of the bottom surface of the package. Gupta contains no disclosure of connecting discs 36 other than by line-like members 32. Contrary to the assertion of the Action, column 1, lines 59-62, and Fig. 1 of Gupta contain no such disclosure. Hence, dependent claim 9 distinguishes over Gupta for this reason in addition to the reasons set forth for independent claim 6. In view of the amendment to claim 9, claim 15 is canceled.

Dependent claim 14 is amended to emphasize another aspect of the invention. Claim 14, as amended, recites:

> the solder lines are formed to a single line-like solder member, *such that each of the terminals is connected to other of the terminals by a single electrical path.*

Reference is made to applicant's Figure 2. The terminals 2 are connected by a single line-like solder member 31. There is only one electrical path between each terminal and the other terminals. This is in contrast to applicant's Fig.1 (corresponding to claim 13, as amended), in which the solder lines are formed in a net-like structure and there are multiple electrical paths connecting each terminal to the other terminals. Gupta discloses a net-like connective structure, but does not disclose a structure as claimed in claim 14 wherein a single line is used and there is only one electrical path between each terminal and the other terminal. Hence, dependent claim 14 distinguishes over Gupta for this reason in addition to the reasons set forth for independent claim 6.

Claim Rejections – 35 USC 103(a)

Claim 10 is rejected under 35 USC 103(a) as obvious over Gupta in view of Duley (USP 5,546,297). Claim 12 is rejected as obvious over Gupta in view of Fujiwara (USP 4,735,847). Duley is cited for its disclosure of sockets and pins. Fujiwara is cited for its teaching of forming a conductive thin film. Neither of these references remedies the deficiencies of Gupta discussed above with reference to Claim 6. Thus, claim 12 is allowable for the same reasons as discussed with reference to claim 6. Claim 10 is canceled, in view of new claims 16-19 which are directed to the socket and pin configuration of applicant's invention. Duley and its relevance to this aspect of applicant's invention will be discussed below.

In addition, with respect to claims 9 and 12, applicant does not assert that the formation of a conductive thin film is novel in itself. Rather, the novelty resides in a method employing the use of a conductive thin film to short circuit terminals of a semiconductor chip package prior to mounting on a circuit board, wherein the film melts away after mounting. Applicant submits that a reference such as Fujiwara, which merely shows use of photolithography and etching to form a conductive thin film, has no bearing on the patentability of the present invention.

New Claims 16-19

New claims 16-19 are directed to the aspect of applicant's invention in which pin-like terminals of a semiconductor package are short-circuited before mounting on a circuit board by wires connecting their tip portions. These wires are cut, and the short-circuited state eliminated, upon insertion of the terminals into the sockets of the circuit board.

Independent claim 16 is not anticipated or rendered obvious by Gupta for the same reasons as discussed with respect to claim 6. In addition, with respect to Duley, applicant does not assert that the mere use of sockets and pins is novel. Rather, the novelty resides in a method employing the use of conductive wires to short circuit the pins prior to mounting on a circuit board, wherein the process of mounting causes the wires to be cut. Applicant submits that a reference such as

Duley, which merely shows use sockets and pins, has no bearing on the patentability of the present invention.

Dependent claims 17-19 are directed to additional details of this aspect of applicant's invention. The wires may be gold wires (claim 17) having a thickness of approximately 70 μm (claim 18). The wires may be fixed to the terminals by an ultrasonic pressure bonding method (claim 19). None of these limitations, in conjunction with the recitations of claim 19, are shown by the references of record.

Conclusion

This application is now believed to be in form for allowance. The examiner is invited to telephone the undersigned to resolve any issues that remain after entry of this amendment. Any fees due in connection with this response may be charged to our Deposit Account No. 50-1314.

Respectfully submitted,
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Date: April 7, 2005

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